REMARKS

Applicants appreciate the Examiner's thorough examination of the present application as evidenced by the Office Action of November 25, 2002 (hereinafter "Office Action"). In response, Applicant has amended independent Claims 10, 15, and 31 to clarify that the isolation layer comprises an insulating material and covers a bottom of the trench.

Applicants respectfully submit that the cited references fail to disclose or suggest the recitations of independent Claims 10, 15, and 31 as amended. Therefore, Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration of all pending claims is respectfully requested for at least the reasons discussed hereafter.

Independent Claims 10, 15, and 31 are Patentable

Claims 10, 15, and 31 stand rejected under 35 U.S.C. §102(e) as being anticipated by U. S. Patent No. 6,184,091 to Gruening et al. (hereinafter "Gruening").

Independent Claim 10 is directed to a method of manufacturing an integrated circuit device in which a trench is formed in a substrate and an isolation layer is formed in the trench. In particular, forming the isolation layer is described as follows:

> forming an isolation layer comprising an insulating material in the trench so as to cover a first sidewall portion of the trench and an entire bottom of the trench;
> ...

Claims 15 and 31 include similar recitations. **FIG. 4**, for example, illustrates this aspect of the present invention by showing the isolation layer 500' disposed in the trench and covering sidewall portions of the trench and the bottom of the trench.

The Office Action cites the filler material **24** shown, for example, in **FIG. 1** of Gruening as corresponding to the isolation layer recited in Claim 10. (Office Action, page 3). In sharp contrast with the isolation layer recited in Claim 10, which is described as comprising an insulating material, Gruening describes the filler material 24 as "a conductive filler material **24**, preferably polysilicon or doped polysilicon..." (Gruening, col. 4, lines 52 - 53). Moreover, as shown in **FIG. 1** of Gruening, the filler material **24** does not cover the entire bottom of the trench as a collar **22** is formed on a portion of the bottom of the trench.

Accordingly, for at least the foregoing reasons, Applicants respectfully submit that

independent Claim 10 is patentable over Gruening, and that dependent Claims 11 - 14 are patentable at least as they depend from an allowable claim.

New Claims 40 - 46 are Patentable

New Claims 40 - 46 have been added that are directed to methods of manufacturing integrated circuit devices in which a mesa structure is formed in a substrate having sidewalls and a top surface. A gate electrode is formed on the mesa structure that extends across the top surface and down respective upper portions of the sidewalls. Applicants respectfully submit that the cited references do not disclose or suggest formation of a gate electrode that extends across the top surface of a mesa structure and down the upper sidewalls of the mesa structure.

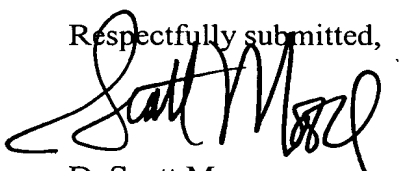
Accordingly, for at least the foregoing reasons, Applicants respectfully submit that independent Claim 40 is patentable and that dependent Claims 41 - 46 are patentable at least as they depend from an allowable claim.

CONCLUSION

In light of the above amendments and remarks, Applicants respectfully submit that the above-entitled application is now in condition for allowance. Favorable reconsideration of this application, as amended, is respectfully requested. If, in the opinion of the Examiner, a telephonic conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (919) 854-1400.

It is not believed that an extension of time and/or additional fee(s)-including fees for net addition of claims-are required, beyond those that may otherwise be provided for in documents accompanying this paper. In the event, however, that an extension of time is necessary to allow consideration of this paper, such an extension is hereby petitioned under 37 C.F.R. §1.136(a). Any additional fees believed to be due in connection with this paper may be charged to our Deposit Account No. 50-0220.

Respectfully submitted,



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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Non-Fee Amendment, Commissioner for Patents, Washington, DC 20231, on February 24, 2003.

Traci A. Brown
Date of Signature: February 24, 2003

VERSION WITH MARKINGS TO SHOW CHANGES MADE

Please amend the following Claims by adding the language that is underlined ("__") and deleting the language that is enclosed within brackets ("[ ]"):

In the Claims:

10. (Amended) A method of manufacturing an integrated circuit device, comprising:

forming a trench in a substrate;

forming an isolation layer comprising an insulating material in the trench so as to cover a first sidewall portion of the trench and an entire bottom of the trench; and

forming a gate electrode on a second sidewall portion of the trench.

15. (Amended) A method of manufacturing an integrated circuit device, comprising:

etching a substrate to form a trench and a mesa therein, the mesa comprising an upper surface and a sidewall, which is adjacent the trench;

filling an entire bottom of the trench with an insulating material so as to cover a first portion of the sidewall and to expose a second portion of the sidewall; and

forming a gate electrode on the second portion of the sidewall and the upper surface.

31. (Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a trench by etching a semiconductor substrate;

partially filling the trench with an isolation layer comprising an insulation material, which leaves upper sidewalls of the trench exposed, but covers an entire bottom of the trench;

forming a gate insulating layer on the upper sidewalls of the exposed trench and an upper surface of the semiconductor substrate adjacent to the trench; and

forming a gate electrode on the gate insulating layer.